IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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INTEGRATED CIRCUIT DEVICE, SYNCHRONOUS-LINK DYNAMIC RANDOM ACCESS MEMORY DEVICE, METHOD OF FORMING AN INTEGRATED CIRCUIT DEVICE AND METHOD OF FORMING A SYNCHRONOUS-LINK DYNAMIC RANDOM ACCESS MEMORY EDGE-MOUNTED DEVICE

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ATTORNEY'S DOCKET NO. MI22-991

INTEGRATED CIRCUIT DEVICE, SYNCHRONOUS-LINK DYNAMIC RANDOM ACCESS MEMORY DEVICE, METHOD OF FORMING AN INTEGRATED CIRCUIT DEVICE AND METHOD OF FORMING A SYNCHRONOUS-LINK DYNAMIC RANDOM ACCESS MEMORY EDGE-MOUNTED DEVICE

TECHNICAL FIELD

The present invention relates to integrated circuit devices, synchronous-link dynamic random access memory devices, methods of forming an integrated circuit device and methods of forming a synchronous-link dynamic random access memory edge-mounted device.

BACKGROUND OF THE INVENTION

Personal computers have experienced expansive growth and improvements in technology in recent decades. Improvements in processing technologies have enabled fabrication of computer components having reduced feature sizes. Such reduction in feature sizes has also enabled the fabrication of smaller components with increased capabilities.

For example, both the operational speeds of processing devices and the capacity to store data of memory devices have been significantly increased. However, there exists a desire to increase the storage capacity of conventional memory devices. Data is stored in components comprising random access memory (RAM) in some conventional configurations. Exemplary random access memory devices include static random access memory (SRAM) and dynamic random access memory (DRAM). It has been desired to increase the speed of memory devices

to increase the overall performance of the conventional computer systems.

Synchronous-link dynamic random access memory (SLDRAM) devices have been introduced to provide faster electronic storage devices. The synchronous-link dynamic random access memory devices provide benefits of very high speed (e.g., 400 megahertz data rate) and very high bandwidth (e.g., 800 Mb/s I/O bandwidth). In addition, such storage devices can provide pipelined or concurrent operation. Exemplary synchronous-link dynamic random access memory devices provide synchronous and packet oriented operation with storage capabilities in excess of 75 MB.

Various packaging configurations have been utilized as housings for conventional synchronous-link dynamic random access memory devices. Exemplary configurations include vertical surface mounted packages (VSMP) and horizontal surface mounted packages (HSMP). In typical configurations, the leads extend from one surface of the mounted packages and are bent and trimmed for the desired orientation.

It has been observed that conventional synchronous-link dynamic random access memory devices produce a considerable amount of heat. Accordingly, various structures have been utilized to reduce or dissipate the generated heat. One prior art technique has considered the utilization of a heat sink bonded to an external wall of a package which houses the synchronous-link dynamic random access memory semiconductor die. In such conventional designs, an epoxy or other

adhesive is typically utilized to bond or otherwise adhere the heat sink to the external surface of the housing package. Drawbacks are presented by the conventional designs inasmuch as subsequent processing of an individual synchronous-link dynamic random access memory device often results in heating the memory device to the point of failure of the epoxy heat sink bond.

Therefore, there exists a need to provide improved memory configurations to overcome the shortcomings experienced within the prior art devices.

SUMMARY OF THE INVENTION

The present invention includes integrated circuit devices, synchronous-link dynamic random access memory devices, methods of forming an integrated circuit device and methods of forming a synchronous-link dynamic random access memory edge-mounted device.

According to one aspect of the present invention, an integrated circuit device includes a semiconductor die and a first housing encapsulating the semiconductor die. A heat sink is positioned proximate the first housing. A second housing is formed to encapsulate at least a portion of the heat sink. The heat sink is preferably thermally coupled with the semiconductor die and configured to dissipate or expel heat therefrom. The second housing is configured to encapsulate both the heat sink and the first housing in certain aspects of the invention.

Another aspect of the present invention provides an integrated circuit device which includes a first housing formed about a semiconductor die and at least portions of a plurality of leads electrically coupled with the semiconductor die. A heat sink is thermally coupled with the first housing. A second housing is formed about the heat sink and at least a portion of the first housing.

The present invention additionally provides methods of forming an integrated circuit device. One aspect provides a method including the steps of providing a semiconductor die and forming a first housing about the semiconductor die. The method also includes thermally coupling a heat sink with the first housing and forming a second housing about at least a portion of the heat sink following the thermally coupling.

The present invention also provides additional structure and methodology aspects.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is an isometric view of a vertical surface mounted package in accordance with the present invention.

Fig. 2 is a side elevational view of a horizontal surface mounted package of the present invention.

Fig. 3 is a top view of a strip of a plurality of first lead frames.

Fig. 4 is a top view illustrating details of one first lead frame of the strip of Fig. 3.

Fig. 5 is an illustrative representation of an exemplary fabrication step of an integrated circuit device.

Fig. 6 is an illustrative representation of another exemplary processing step subsequent to the step shown in Fig. 5.

Fig. 7 is a side elevational view of an integrated circuit package at an intermediate processing step.

Fig. 8 is a top view of a second lead frame.

Fig. 9 is a side elevational view of a heat sink of the second lead frame positioned adjacent a first housing.

Fig. 10 is a side elevational view of an integrated circuit device according to a first embodiment of the present invention.

Fig. 11 is a side elevational view of an integrated circuit device according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, an integrated circuit device 10 according to the present invention is illustrated. The described embodiment discloses a synchronous-link dynamic random access memory (SLDRAM) edge-mounted device. The depicted integrated circuit device 10 comprises a

vertical surface mounted package (VSMP). A horizontal surface mounted package (HSMP) is also provided in other embodiments. The embodiments depicted herein are exemplary. The present invention is not limited to such disclosed arrangements but can be utilized with other integrated circuit device configurations.

The illustrated integrated circuit device 10 includes a housing 11 provided about an internal semiconductor die 15 and a heat sink 17. As described below with reference to Fig. 2, housing 11 can include a first housing portion and second housing portion (only the second housing portion is visible in Fig. 1). In accordance with the presently described embodiment, semiconductor die 15 comprises synchronous-link dynamic random access memory circuitry. Semiconductor die 15 can be configured to provide additional and/or other functions.

A plurality of leads are coupled with one end of housing 11. In particular, the illustrated leads comprise plural first leads 14 coupled with the internal semiconductor die 15 and plural second leads 16 coupled with heat sink 17. First leads 14 are operable to provide electrical interconnection of semiconductor die 15 with external circuitry (not shown). Second leads 16 are operable to expel, dissipate or otherwise conduct heat generated within integrated circuit device 10 to external components, such as an externally provided heat sink (not shown). First leads 14 and second leads 16 are arranged to provide an integrated circuit device configuration which can be mounted in a vertical orientation.

Referring to Fig. 2, another configuration of integrated circuit device 10a is shown. Like numerals represent like components with any significant differences therebetween being represented by the suffix "a." Integrated circuit device 10a is configured as a horizontal surface mounted package. Similar to the vertical surface mounted package depicted in Fig. 1, integrated circuit device 10a is configured to house semiconductor die 15 and heat sink 17.

First and second leads 14a, 16a are bent or otherwise configured to provide horizontal mounting of integrated circuit device 10a. Leads 14a are configured to provide electrical connection with external electrical couplings (not shown). Second leads 16a are configured to provide coupling of internal heat sink 17 with an external thermal conductor (not shown).

Housing 11 can comprise the same housing configuration in both devices depicted in Fig. 1 and Fig. 2. The depicted housing 11 includes a first housing portion 12 and a second housing portion 13. First housing portion, also referred to as a first housing 12, is formed about semiconductor die 15 and at least a portion of first leads 14a. Second housing portion, also referred to as a second housing 13, is formed about at least a portion of heat sink 17 and at least a portion of second leads 16a.

More specifically, first housing 12 is configured to encapsulate or otherwise house semiconductor die 15 and at least a portion of first leads 14a in the illustrated embodiment. Second housing 13 is

configured to encapsulate or otherwise house heat sink 17, first housing 12 and at least a portion of second leads 16. Second housing 13 also encapsulates at least a portion of first leads 14 in the depicted embodiment.

Referring to Fig. 3 - Fig. 6, exemplary process steps for fabrication of first housing 12 are illustrated. Other and/or additional process steps can be utilized to fabricate first housing 12 of integrated device 10 in accordance with other fabrication methodologies.

Referring specifically to Fig. 3, a lead frame strip 20 is diagrammatically and in broad outline illustrated. Lead frame strip 20 comprises a plurality of first lead frames 22 provided thereon. First lead frames 22 are individually configured to couple with and support a semiconductor die. First lead frames 22 can comprise a thin conductive metal such as copper. Lead frame strip 20 is utilized to simultaneously fabricate a plurality of integrated circuit devices.

Referring to Fig. 4, details of an exemplary first lead frame 22 are illustrated. Semiconductor die 15 is illustrated coupled with first lead frame 22 in Fig. 4. In the described embodiment, first lead frame 22 includes plural first leads 14 operable to provide electrical connection with semiconductor die 15.

First lead frame 22 additionally includes a pad 24 configured to provide a mounting surface for semiconductor die 15 (a portion of pad 24 is provided below semiconductor die 15 and is not visible in the depicted arrangement). Semiconductor die 15 can be mechanically

bonded to pad 24 using an epoxy. Other attachment methods of semiconductor die 15 can be utilized. Pad 24 is coupled with and supported by external portions of first lead frame 22 via plural lead frame supports 26.

The depicted semiconductor die 15 includes a plurality of bond pads 30. Following mechanical bonding or other coupling of semiconductor die 15 with pad 24 of first lead frame 22, wire bonding connections 32 are formed to couple individual bond pads 30 with corresponding first leads 14. Wire bonding connections 32 individually comprise gold in the described embodiment. Wire bonding connections 32 are operable to provide electrical coupling of first leads 14 with respective bond pads 30 and internal circuitry of semiconductor die 15. Alternative electrical connection methods of leads 14 and semiconductor die 15 are possible.

Referring to Fig. 5 and Fig. 6, additional exemplary fabrication steps of integrated circuit device 10 are described. As shown in Fig. 5, first lead frame 22 having semiconductor die 15 mounted thereon is placed within a mold 40. As illustrated, mold 40 comprises opposing first and second forms 44, 46. Mold 40 is configured in the described fabrication method to form first housing 12. In particular, first lead frame 22 comprising first leads 14 and pad 24 and semiconductor die 15 are provided intermediate opposing forms 44, 46 of mold 40. Forms 44, 46 include respective dams 48, 50. Lead frame 22 and

semiconductor die 15 are preferably aligned with dams 48, 50 as shown in Fig. 5.

Mold 40 also provides a defined volume 41 intermediate forms 44, 46. A tablet of powdered resin 42 is placed within mold volume 41 and intermediate forms 44, 46. Resin 42 is inserted within volume 41 to provide material to form first housing 12 to house semiconductor die 15. A plunger 43 is positioned adjacent volume 41. Plunger 43 is operable to move upwardly to force resin 42 toward semiconductor die 15 and lead frame 22 positioned within mold 40.

Referring to Fig. 6, following placement of semiconductor die 15 and lead frame 22 within mold 40, forms 44, 46 are brought together. Respective dams 48, 50 define an inner chamber 52. Chamber 52 is configured to define the perimeter of first housing 12. Forms 44, 46 also define a runner 54 intermediate volume 41 and chamber 52. Volume 41 has been substantially filled with plunger 43 in Fig. 6. Runner 54 and chamber 52 have been substantially filed with resin 42 in Fig. 6.

Lead frame 22 and semiconductor die 15 are aligned within chamber 52 defined within mold 40. Following closure of forms 44, 46, mold 40 can be heated to an increased temperature, such as 180° C. Heating of mold 40 results in melting of resin 42 within the tablet. Plunger 43 can be utilized to force the melted resin 42 through runner 54 into chamber 52. The melted resin 42 fills chamber 52 as

shown. Thereafter, resin 42 is permitted to sufficiently solidify or otherwise cure within mold 40 to form first housing 12.

Referring to Fig. 7, first housing 12 and the first lead frame (not shown in Fig. 7) are removed from the mold following sufficient solidification of resin 42. As shown, resin 42 encapsulates semiconductor die 15, lead frame pad 24, wire bonding connections 32, and a portion of first leads 14. Unencapsulated portions of first leads 14 are exposed outside of first housing 12.

First housing 12 can be removed from the first lead frame following removal of first housing 12 and the first lead frame from mold 40. In particular, pad connections 26 (shown in Fig. 4) are broken to remove first housing 12. Thereafter, first housing 12 can undergo further processing to form the desired integrated circuit device 10.

Referring to Fig. 8, a second lead frame 60 is illustrated. Second lead frame 60 includes heat sink 17. Second lead frame 60 is formed of a thermally conductive material such as a metal in the described embodiment. Heat sink 17 includes a body 18. Heat sink body 18 is supported by plural supports 62. The illustrated heat sink 17 includes plural second leads 16 coupled with heat sink body 18. Second lead frame 60 is typically provided within a lead frame strip (not shown) similar to first lead frame strip 20 shown in Fig. 3. Such a strip could include a plurality of heat sinks 17 corresponding to the number of first lead frames 22 provided.

Referring to Fig. 9, following sufficient solidification of first housing 12 and removal thereof from the first mold and the first lead frame, heat sink 17 of second lead frame 60 is thermally coupled with first housing 12. In the described embodiment, heat sink 17 is positioned proximate or adjacent first housing 12. In the preferred embodiment, heat sink 17 is positioned against or in contacting relation with first housing 12. Heat sink 17 is configured to draw heat generated from semiconductor die 15 and preferably expel or dissipate the heat.

The second housing of the integrated circuit device is thereafter formed. Although not illustrated, the method of forming the first housing can be utilized to form the second housing. Such can be referred to as a "double molding" process. More specifically, following the positioning of heat sink 17 against first housing 12, or other suitable thermal coupling, second lead frame 60 and first housing 12 are provided within a second mold. Such a mold contains appropriate forms having dams to define a second chamber for forming the second housing of the integrated circuit device.

A resin tablet is inserted into the second mold and first housing 12 and second lead frame 60 are placed within the appropriate second chamber formed within the second mold. The second mold is subsequently heated to a sufficient elevated temperature to melt the resin. Thereafter, a plunger is utilized to force the melted resin into

the second chamber containing first housing 12 and second lead frame 60.

The resin is thereafter permitted to sufficiently solidify to form the second housing. First and second housings 12, 13 (shown in Fig. 10) are removed from the mold following such solidification. Second housing 13 is then removed from second lead frame 60 by breaking connections 62 (shown in Fig. 8). Connections 62 are broken to free heat sink 17 and second housing 13 from lead frame 60.

Referring to Fig. 10 and Fig. 11, plural housing configurations 11, 11a of respective integrated circuit device configurations 10, 10b are illustrated. Fig. 10 and Fig. 11 individually illustrate respective integrated circuit devices 10, 10b at a step following the removal of devices 10, 10b from the second lead frame. Devices 10, 10b are depicted at a step prior to final fabrication steps comprising bending and trimming of first leads 14 and second leads 16 which extend from the illustrated housings 11, 11a.

Referring specifically to Fig. 10, the first configuration of housing 11 is shown. First housing 12 of housing 11 is formed about semiconductor die 15 and at least portions of leads 14 coupled with semiconductor die 15. Second housing 13 is formed about at least a portion of first housing 12, at least a portion of first leads 14 and at least a portion of heat sink 17.

In particular, first housing 12 and second housing 13 individually comprise encapsulant housings in the configuration shown in Fig. 10.

More specifically, first housing 12 encapsulates semiconductor die 15 and at least a portion of first leads 14. Second housing 13 encapsulates a majority of heat sink 17 and a majority of first housing 12. More specifically, second housing 13 encapsulates first housing 12, heat sink body 18, and at least a portion of first leads 14 and second leads 16.

Referring specifically to Fig. 11, another configuration of housing 11a of integrated circuit device 10b is illustrated. In the depicted configuration, first housing 12 encapsulates semiconductor die 15 and a portion of first leads 14. Second housing 13a is shown provided about at least a portion of heat sink 17 and first housing 12. In particular, second housing 13a is shown encapsulating three surfaces of heat sink body 18 and a portion of first housing 12 in the configuration depicted in Fig. 11.

Other housing configurations of integrated circuit device 10 can be formed according to the present invention. First housing 12 can be provided about or configured to encapsulate more or less components of integrated circuit device 10. Further, more or less portions of first housing 12 and heat sink 17 can be encapsulated or otherwise covered by second housing 13.

External exposed portions of first leads 14 and second leads 16 can be trimmed and/or bent into appropriate positions to provide the desired integrated circuit device 10, 10a forming a vertical surface mounted package or a horizontal surface mounted package as depicted in Fig. 1 and Fig. 2, respectively.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.